CLAIMS

1. A computer program on a media usable with a computer for testing combinational and sequential logic circuits where memory units are coupled together to form shift register latches that are arranged in a shift register scan path with an input and output for testing the logic circuits, said computer program comprising:

load pattern computer code for shifting data through the scan path to load the shift register latches with a first data pattern representative of a stuck-at fault condition;

pattern variation computer code for causing permutation of at least one of the following operating parameters: a supply voltage, a reference voltage, a timing pattern temperature and a timing sequence to trigger a change in state of at least one of the memory units in the shift register scan path; and

analyzing computer code for determining the memory unit furthest from the shift register scan path output that has changed state from its loaded value.

2. The computer program of claim 1, wherein said pattern variation computer code is for causing permutations in a plurality of the operating parameters.

3. The computer program of claim 2, wherein said analyzing computer code includes shifting code for shifting data out of the scan path after each of the operating parameters is separately permuted.

4. The computer program of claim 3, wherein said analyzing computer code includes selection computer code for selecting the last bit read out that has changed from its load pattern as being from the shift register latch closest to the stuck-at fault memory unit.

5. A method for testing combinational and sequential logic circuits where memory ;units are coupled together to form shift register latches, arranged in a shift register scan path with an input and output for testing the logic circuits, the method comprising:

shifting data through the scan path to load the shift register latches with a first data pattern representative of a stuck-at fault condition;

causing permutation of at least one of the following operating parameters: a supply voltage; a reference voltage; a timing pattern temperature and a timing sequence to trigger a change in state of at least one of the memory units in the shift register scan path; and

determining the memory unit furthest from the shift register scan path output that has changed state from its loaded value.

6. The method of claim 5 including:

causing permutations in a plurality of the operating parameters.

7. The method of claim 6 including:

shifting data out of the scan path after each of the operating parameters is separately permuted.

8. The method of claim 7 including:

the last bit read out that has changed from its load pattern as being from the shift register latch closest to the stuck-at fault memory unit.